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Field enhanced blockade of the confined energy levels in nanometer scale pillar arrays

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Abstract

We report observations of dramatic hysteretic switching behavior in nanometer scale pillar arrays. Using a new technique, we fabricate arrays of closely packed pillars 20–50 nm in diameter from a GaAs/AlAs resonant tunneling diode heterostructure. The array resistance switches between two stable states with a current peak to valley ratio of 500:1. Scanning tunneling microscope characterization of individual pillars suggests that the pillars trap charge to block the flow of current through the quantum confined states.

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Electron transport through laterally confined resonant tunneling diodes [1] (RTDs) can be influenced by both Coulomb charging [2,3] and low-dimensional quantum size effects [4]. In a laterally confined RTD, a quantum dot is formed by etching a double barrier heterostructure into a submicron diameter pillar. In principle, charging and quantum confinement energies can be increased by simply reducing the pillar dimensions. In practice, there has been a limit to the minimum device diameter due to the presence of surface states which deplete the electron channel, and block current flow [5].

We have characterized arrays of nanometer scale RTD pillars and observe behavior which suggests that surface charge trapping can be used controllably, to gate current flow. Measurements of more than 10^5 RTD pillars in parallel reveal that the array resistance switches between two stable states with a current peak to valley ratio of 500:1. Scanning tunneling microscope characterization shows that an individual pillar traps charge to change the position of the quantum confined states with respect to the conduction band. These results imply that in the array, the resistance switches due to the simultaneous charging of the individual pillars.

The nanoscale pillar arrays are made using a "natural" lithographic technique [6]. First, we evaporate a thin gold film onto the semiconductor surface. It is well documented that for film thickness

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less then around 10 nm, gold forms a granular layer composed of disconnected islands [7]. The gold islands partially mask the underlying material so that plasma etching in a $SiCl_4$/Ar environment selectively removes the material between the islands and produces an array of semiconductor pillars. Fig. 1a shows a transmission electron micrograph of a typical sample after etching. The pillars are densely packed with diameters ranging from 20–50 nm and with an etch depth of approximately 320 nm. The dark bands visible in the micrograph show the strain caused by the etching process which leaves the pillars bent about 5° off normal.

Our device is drawn schematically in Fig. 1b [8]. An RTD pillar array is formed by etching a double barrier AlAs/GaAs heterostructure in the manner described above. In our structure, a 5.6 nm thick GaAs well is isolated between 2 nm thick AlAs barriers. The GaAs leads are Si doped n-type, with a concentration graded from 5×10^{18} cm^{-3} at the contacts to 2×10^{17} cm^{-3} near the barriers. Contact is made to the top of the pillars by evaporating a 30×30 micron gold pad. The gold pad does not fill the gaps between the pillars because the gold grain size is approximately the same as the pillar spacing. A Si_3N_4 insulating layer is used to support the wire bond. The back contact is AuGeNi annealed at 400°C for 10 s.

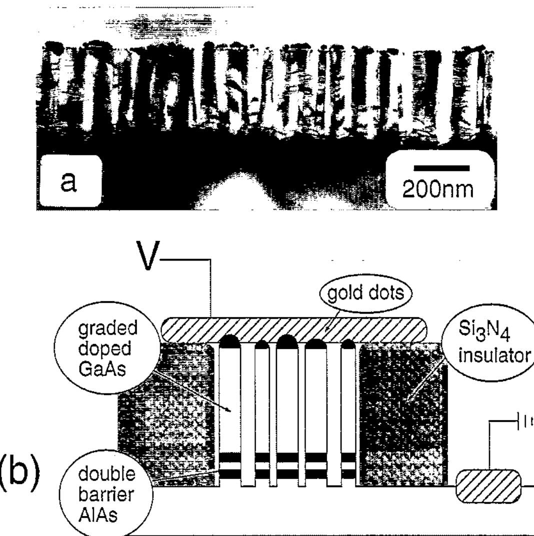

Fig. 1. (a) Transmission electron micrograph of a typical pillar array sample. The Au mask is 5 nm thick and the sample was etched for 3 min in 10 mTorr $SiCl_4$:Ar at a ratio of 1:2 with a power density of 4 mW/cm^2. (b) Schematic drawing of the resonant tunneling diode pillar array device.

Fig. 2 shows the result of a typical hysteresis measurement made at room temperature. Starting at zero bias, the device is initially in a high resistance state. Moving to negative bias, the current jumps sharply to a low resistance state at −2.4 V. The device stays in the low resistance state until the bias crosses zero and increases to +1.4 V. Here the device switches back to the high resistance state with a current peak to valley ratio of 500:1. Further measurements show that the high resistance state remains stable at zero bias for an unlimited period of time while the low resistance state is stable for at least one hour before eventually switching to the high resistance state. In comparison, measurements of a standard 10 micron diameter RTD made from the same material showed a room temperature peak to valley ratio of only 3:1 and no hysteretic switching behavior [9]. Switching was observed in pillar arrays fabricated from two double barrier wafers which were obtained from separate growth facilities.

Because the pillars are small and closely packed, it is impossible to contact a single device by conventional means. However, using a scanning tunneling microscope (STM), we are able to locate and contact isolated pillars. Our measurements are done using a tungsten tip WA Technology STM operating at room temperature in air. We first locate an individual pillar by measuring the tunnel

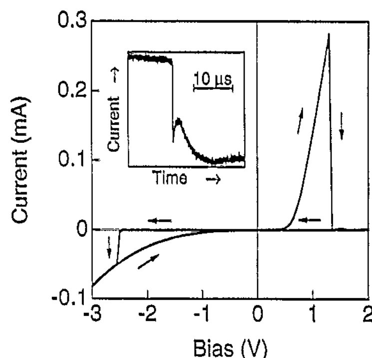

Fig. 2. Current versus source–drain bias for a typical resonant tunneling diode pillar array device. The peak to valley ratio is 500:1. The inset shows the current as a function of time as the device switches between the low and the high resistance state.

gap required to provide constant current while scanning the tip along the sample surface. Once a pillar is located, the gap is reduced bringing the tip in light contact with the sample. If we retract the tip, our original scan can be reproduced, demonstrating that the surface is not damaged by the process. A number of pillars giving similar results were measured in this way.

Fig. 3a shows the current–voltage characteristics of a 40 nm diameter RTD pillar measured with an STM tip contact. The trace is hysteretic: negative differential resistance (NDR) is observed when the bias starts at zero and is swept to a higher positive or negative value; NDR is not observed in the opposite sweep direction. Reproducible results are obtained for a constant sweep rate, but the peak to valley ratio decreases as the sweep rate is decreased.

To explain these results, we propose that trapped charge modifies the position of the conduction band in the center of the pillar [5]. One possible mechanism is seen in Fig. 4. On the surface of the

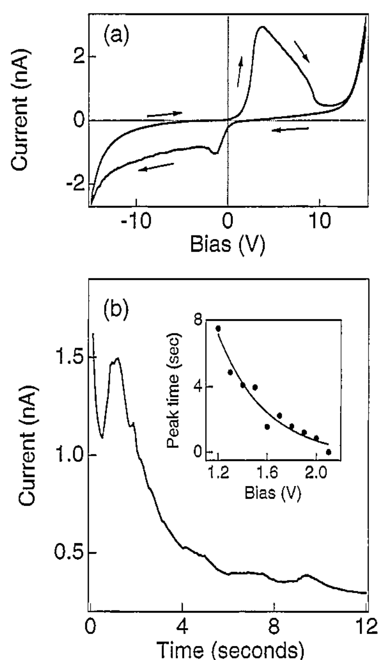

Fig. 3. (a) Current–voltage characteristic of a 40 nm diameter RTD pillar measured with an STM tip contact. The sweep rate is 200 mV/s. (b) Current as a function of time as the pillar recharges. The inset shows the position of the main peak for different recharging biases (see text). The solid line is a guide to the eye.

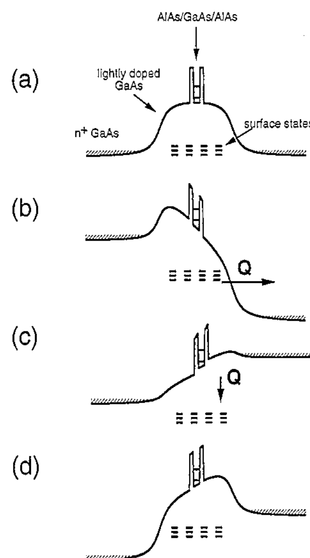

Fig. 4. Schematic drawing of the charge gating mechanism. (a) At equilibrium, the surface states are pinned at the Fermi energy creating a depletion barrier in the lightly doped region. (b) Large applied bias causes charge to tunnel from the surface states into the drain. The empty positively charged states pull down the conduction band near the well. (c) As the states recharge at low bias, the conduction band rises. (d) Eventually, the device returns to the steady state.

pillar, a large density of localized states exist due to dangling bonds and strain. In equilibrium, (Fig. 4a), the Fermi energy E_F is pinned within these surface states. This depletes the electron density in the center of the pillar and forms a large barrier in the central lightly doped region. When a large bias is placed on the device, (Fig. 4b), electrons are forced out of the surface states, creating a net positive charge Q. This positive charge acts as a gate to reduce the level of the central barrier, and thus also the relative energies of the electron states confined in the well. Experimentally, NDR occurs in the forward sweep direction as the conduction band energy E_c moves above the well resonance with increasing bias. But as the bias is swept back to zero, electrons have not yet repopulated the surface states and the resonance level stays pinned below E_c.

The charge gating effect can be observed more directly by monitoring the current as a function of time while the pillar recharges. The results of this experiment are shown in Fig. 3b. The device is

biased at -15 V for 10 s (Fig. 4b), after which the current is plotted as a function of time while the device recharges at $+1.9$ V. A strong peak is observed on top of a slow decay in the current. As seen in Fig. 4c, when the bias is switched to the recharging voltage, the quantum well resonance initially lies below E_c. As the surface states slowly return to their equilibrium value, the resonance state rises, and moves through E_c (Fig. 4d). This appears as a peak in Fig. 3b. If we change the bias, we expect this will influence the recharging time, and thus move the peak position. In the inset, the peak is observed to occur sooner for larger biases, as expected for a faster recharging time.

We now consider the influence of charge gating on the large area device. Here, a sharp transition is observed between the high resistance and the low resistance state (Fig. 2). In the high resistance state, (Fig. 4a), current is blocked by the depletion region which forms around the barrier structure due to the negatively charged surface states. Upon application of reverse bias, electron charge is forced from the surface states, lowering the depletion region barrier (Fig. 4b). A sharp switch to the low resistance state eventually occurs when E_c in the depletion region is pulled below E_F.

In the low resistance state, the surface states are positively charged, and remain trapped below E_c in a quasi-stable situation. If positive bias is applied, the quantum well resonance eventually passes E_c. This switches the device off, and induces the surface states to return to the equilibrium level. Evidence for this resonant induced mechanism is provided by time dependent measurements of the large area device as it switches from the low to the high resistance state. As shown in the inset to Fig. 2, the switch occurs in less than 10^{-7} s, and is followed by a slow rise and then decay in the current. We attribute the initial switch to the confined level in the quantum well, while the slow rise and decay (as also seen in Fig. 3b) is due to the charging of the surface states.

Admittedly, this model does not completely describe the behavior of the large area device. It is still unclear why the positively charged state remains stable for so long, and why the resonance switch causes simultaneous repopulation of the trapped states. This is in contrast to an individual pillar, where more gradual charging is observed. An additional complication is that recently similar results have been observed in single barrier material (although no switching is observed in pillars with no barrier). This suggests that double barrier confinement is not crucial to observe the switching behavior. To explain the fast switch, a more detailed analysis is needed which perhaps takes into account interactions among the pillars.

In conclusion, we have observed dramatic hysteretic switching behavior at room temperature in resonant tunneling pillar arrays. STM measurements of individual pillars suggest that this effect is caused by the charging and de-charging of trap states which influence the energy of the confined levels. We hope that further experiments will lead to a more complete theory to describe the observed behavior.

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