Resistance bi-stability in resonant tunneling diode pillar arrays

B. W. Alphenaar,[a] Z. A. K. Durrani, A. P. Heberle, and M. Wagner
Hitachi Cambridge Laboratory and University of Cambridge Microelectronics Research Centre, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, United Kingdom

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We have fabricated and characterized resonant tunneling diode pillar arrays. The array resistance switches between two stable states with a maximum room temperature current peak to valley ratio of 500:1. Both the high and the low resistance states are stable at zero bias suggesting that the device may be used for non-volatile memory storage. © *1995 American Institute of Physics.*

Resonant tunneling diodes (RTDs) are one of the most promising quantum effect devices for practical applications.[1] The presence of negative differential resistance at room temperature[2] allows RTDs to be used as memory storage devices. Recent work has demonstrated that the buildup of electron charge in the well can have a strong influence on the bias required to switch between stable states.[3] In addition, single electron charging effects become pronounced as the size of the device is reduced.[4] For asymmetric barriers the tunneling characteristics of a quasi-one-dimensional RTD at low temperature can be completely dominated by electron charging.[5]

To study the influence of electron charging on small scale RTDs we have produced a new type of device consisting of an array of randomly sized RTD pillars. Each pillar is less than 50 nm in diameter so that the single electron charging energy for tunneling into the well is expected to approach kT at room temperature. When measured in parallel, the pillars show switching between a low and a high resistance state with a maximum room temperature peak to valley current ratio of 500:1. Both resistance states are stable with zero-bias on the device, suggesting that the device may be used for non-volatile memory storage.

We fabricate our samples using a natural lithographic process.[6] First, we evaporate a thin gold film onto the semiconductor surface. It is well documented that for film thicknesses less than around 10 nm, gold forms a granular layer composed of disconnected islands.[7] The gold islands partially mask the underlying material so that plasma etching in a $SiCl_4$/Ar environment selectively removes the material between the dots and produces an array of semiconductor pillars. Figure 1 shows an electron beam micrograph of a typical sample surface after etching. Here, an array of randomly shaped pillars 350 nm high and 20–50 nm in diameter is seen. Some of the pillars are partially connected to form larger structures. The pillar array uniformly covers the vast majority of a 5×5 mm sample surface.

Our device is drawn schematically in Fig. 2. A RTD pillar array is formed by etching a double barrier AlAs/GaAs heterostructure in the manner described above. A top contact to the pillar array is made by evaporating a 30×30 micron gold pad. The contact pad does not fill the gaps between the pillars because the grain size of the gold (20–50 nm) is approximately the same as the pillar spacing. The back contact is AuGeNi annealed at 400 °C for 10 s. The light and dark characteristics of more than 50 such devices were measured at room temperature using a standard probe station. In each case, qualitatively similar results were obtained.

Figure 3 shows the result of a typical hysteresis measurement. Starting at zero bias, the device is initially in a high resistance state. Moving to negative bias, the current jumps sharply to a low resistance state at -2.4 V. The device stays in the low resistance state until the bias crosses zero and increases to 1.4 V. Here, the device switches back to the high resistance state with a current peak to valley ratio of 500:1. In comparison, measurements of a standard 10 μm diameter RTD made from the same material showed a room temperature peak to valley ratio of 3:1 and no hysteretic switching behavior.[8] The peak current density of the pillar array is approximately 50% of the standard RTD. Breakdown occurs for biases above approximately ±10 V, afterwhich no further switching is observed.

To test the stability and reproducibility of the RTD pillar array device, we performed a series of hysteresis measurements. The results of this test for two different devices is shown in Fig. 4. Here the current in the low resistance state (peak current) is compared with the current in the high resis-

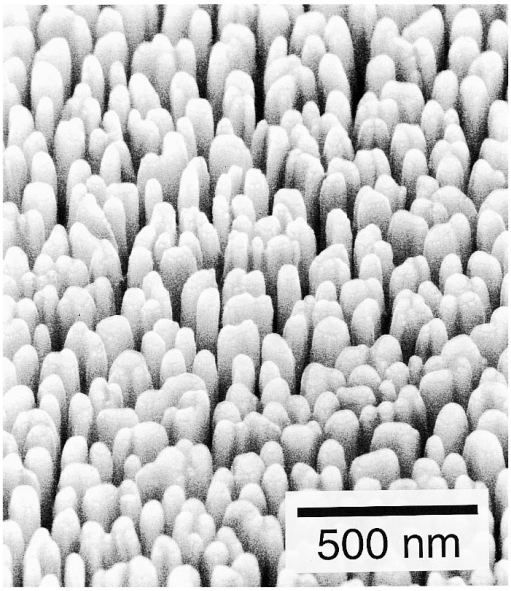

FIG. 1. Electron beam micrograph of a typical pillar array sample. The Au mask is 5 nm thick and the sample was etched for 3 minutes in 10 mTorr $SiCl_4$:Ar at a ratio of 1:2 with a power density of 4 mW/cm^2.

[a]Electronic mail: alphenaar@phy.cam.ac.uk

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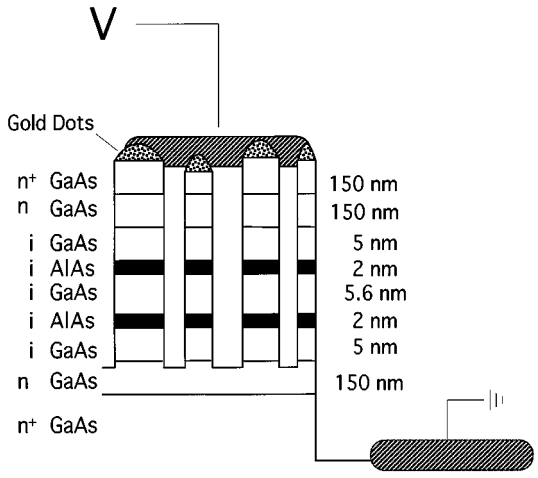

FIG. 2. Schematic drawing of the RTD pillar array device. The drain contact is AuNiGe.

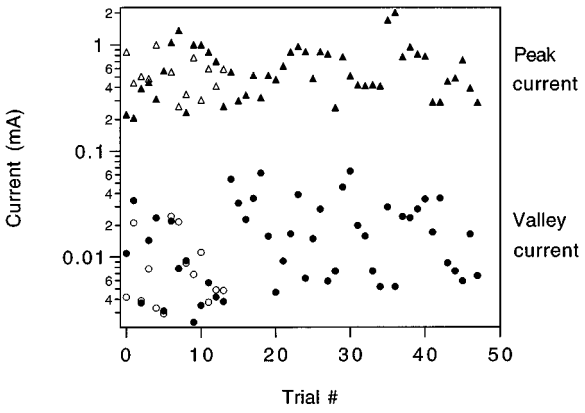

FIG. 4. Peak current (triangles) and valley current (circles) measured at 1 V for successive switches between the low and the high resistance states. The voltage is swept between −5 and + 2 V at a sweep rate of 50 mV/sec. Two different devices (solid and open symbols) are compared. Note that the current is plotted on a log scale.

tance state (valley current) measured at a bias of 1 V following a particular switching event. The first device (solid triangles and circles) shows a large variability in both the peak and the valley currents. However, the peak to valley ratio never drops below 5:1, and sometimes is as high as 400:1. After 50 trials, no degradation in device performance is observed. A second device (open triangles and circles) was tested for comparison over 13 trials. The peak and valley currents lie within the same set of values as the first device, and once again no degradation is observed.

The RTD pillar array can be used as a zero-bias two-terminal memory device: the low resistance state represents one stored bit of information which can be erased by switching the device to the high resistance state. This process is demonstrated in Fig. 5. Starting at zero bias in the low resistance state [Fig. 5(a)], the device switches to the high resistance state at 1.7 V. This corresponds to erasing the previously stored information. Afterwards, the state of the device can be probed by applying a positive voltage and measuring the resistance. This is seen in Fig. 5(b), where the current remains low as the bias is increased, after being at 0 V for 10 min. The information can be re-stored by applying a large enough negative bias, which switches the device to the low resistance state. Figure 5(c) shows the same trace taken after pulsing the device with −5 V for 1 s. The original characteristics [Fig. 5(a)] are reproduced. Further measurements show that the high resistance state remains stable at zero bias for an unlimited time while the low resistance state is stable for at least 1 hour before eventually switching to the high resistance state.

We are still developing a detailed theory to describe the switching behavior. Clearly, trapped charge—either in the well or in surface states surrounding the well—has a strong influence on the energy of the resonant level. In the low resistance state the resonant level is accessible, however, as the bottom of the conduction band moves through the resonance energy, the trapped charge escapes. This switches the device to the high resistance state. If the switching behavior is due to a resonant process we expect that the switching time should be similar to that observed in a typical resonant tunneling device. In Fig. 6 we show the current as a function of time as the device switches from the low to the high resistance state. The switch occurs in less than 10^{-7} s and is

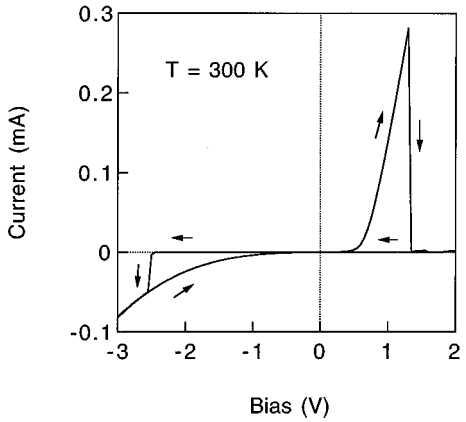

FIG. 3. Current versus source-drain bias for a typical RTD pillar array device. The peak to valley ratio is 500:1.

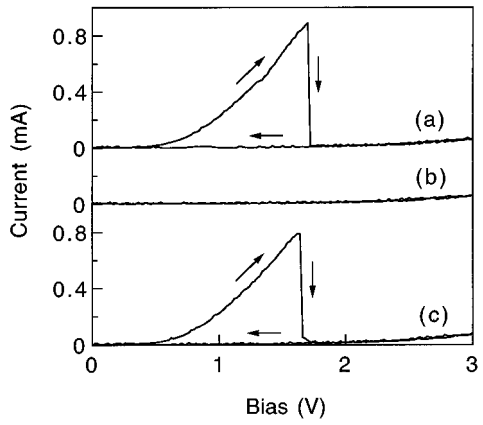

FIG. 5. Current versus source-drain bias for the pillar array acting as a memory storage device. (a) The device, originally in the on state at 0 V, switches to the off state at 1.7 V. (b) The device stays in the off state if the bias remains positive. (c) After pulsing the bias at −5 V for one second, the device returns to its original state.

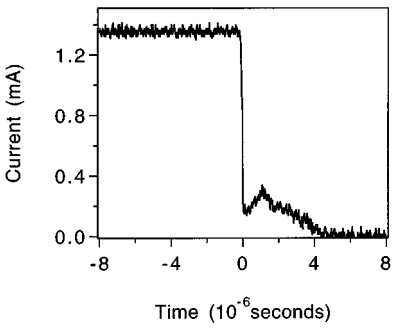

FIG. 6. Current as a function of time as the device switches between the low and the high resistance state.

followed by a slower exponential decay. This suggests an initial resonant switch followed by a slower decharging of the trapped states.

In conclusion, we have observed dramatic hysteretic switching behavior at room temperature in resonant tunneling pillar arrays. The peak to valley current ratio can be as high as 500:1 and both the high and low current states are stable with zero bias on the device. We hope that further experiments will lead to a more complete theory to describe the observed behavior.

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