Operation of logic function in a Coulomb blockade device

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(Received 6 August 1998; accepted for publication 24 August 1998)

This letter presents the experimental demonstration of a Coulomb blockade (CB) logic device. Our logic architecture consists of an array of current pathways, controlled by CB switching nodes. In this architecture, high gain is not required to transmit information, making it well suited to the CB device. Each CB node is switched between a blockaded state and a completely pinched-off state, minimizing the influence of stray potentials. Using a multi-phase clocking scheme to precisely control electron flow, the AND logic function is observed using as few as 160 electrons. © *1998 American Institute of Physics.* [S0003-6951(98)01043-2]

Power consumption has become a limiting factor in the evolution of semiconductor microprocessors. Due to miniaturization and improved operation methods, the average power consumption per transistor within a state-of-the-art microprocessor has decreased by a factor of 2 over the last 5 years. During this same time, though, the number of transistors per microprocessor has increased rapidly, so that the total power consumption per microprocessor has gone up by a factor of 3.5. To decrease power consumption, the number of electrons used to switch each transistor between its ON and OFF states (currently 100 000) should be reduced. If the number of electrons becomes too small, however, charge fluctuations will produce unacceptable variations in the threshold current. Recently, the Coulomb blockade (CB) effect has been promoted as a possible means by which to control such charge fluctuations.[1–13] The CB effect can be observed most directly in the single electron tunneling (SET) transistor, which consists of a small gated island connected by tunnel barriers to source and drain leads. If the charging energy of the island is much larger than the thermal energy, current flow through the device can be blocked by the presence of a single excess electron on the island.[1,2] At cryogenic temperatures, the accuracy of the CB effect in transferring single electrons approaches the metrological level.[3]

Much effort has gone towards incorporating CB effects in memory devices,[4] and recently, switching between CB cellular automata has been demonstrated.[5] In addition, many logic devices based on SET have been proposed,[6,7] but due to practical problems, none has yet been realized. The main failing of the SET for logic applications is that it is too easily influenced by stray voltages within the surrounding logic circuitry. Because the SET is sensitive to the charge of one electron, only a small fluctuation in the background potential is needed to move it away from the blockaded state. Also, standard logic devices rely on the high gain of the metal–oxide–semiconductor (MOS) transistor to allow fan out of information among the logic components without undue loss. By comparison, the gain of the SET is very small.[8]

In this work, we demonstrate a CB logic device in which these problems have been circumvented. Our method is to use an architecture based on the binary decision diagram (BDD)[14,7] [Fig. 1(a)]. The BDD consists of an array of possible current paths, connected by two-way switching nodes. The nodes do not need high gain, but only a distinct ON–OFF switching characteristic.

The BDD diagram shown in Fig. 1(a) describes the digital function AND. The two switches X_1 and X_2 form decision making nodes at the intersections of the current paths.[11] A packet of electrons starting from the root, can either take path 0 or path 1. If both nodes X_1 and X_2 are in the 1 position, the electron packet will arrive at leaf 1 (the result $X_1 \cdot X_2$). If either X_1 or X_2 is 0, the electron packet will arrive at leaf 0 (the result $\overline{X_1 \cdot X_2}$). The structure thus distinguishes $X_1 = 1$ AND $X_2 = 1$ from all other cases. By different definitions to the variables and leaves in this structure, NAND, OR, and NOR functions can also be realized, and by combinations of the varied structures, any other logic function can be created. Our BDD AND device is made using

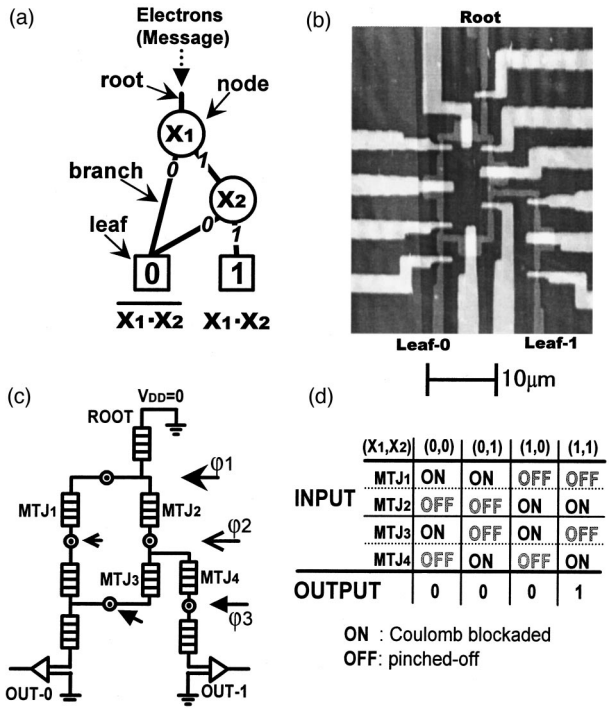

FIG. 1. (a) A BDD diagram representing the AND logic function. (b) AFM image of the AND function device. Ti/Au Schottky gates cover the 0.3 μm wires to form MTJs. Gates on the wide pads are used for the clocking pulses. (c) An equivalent circuit of the device including measurement equipment. (d) Truth table relating input to output for the AND device.

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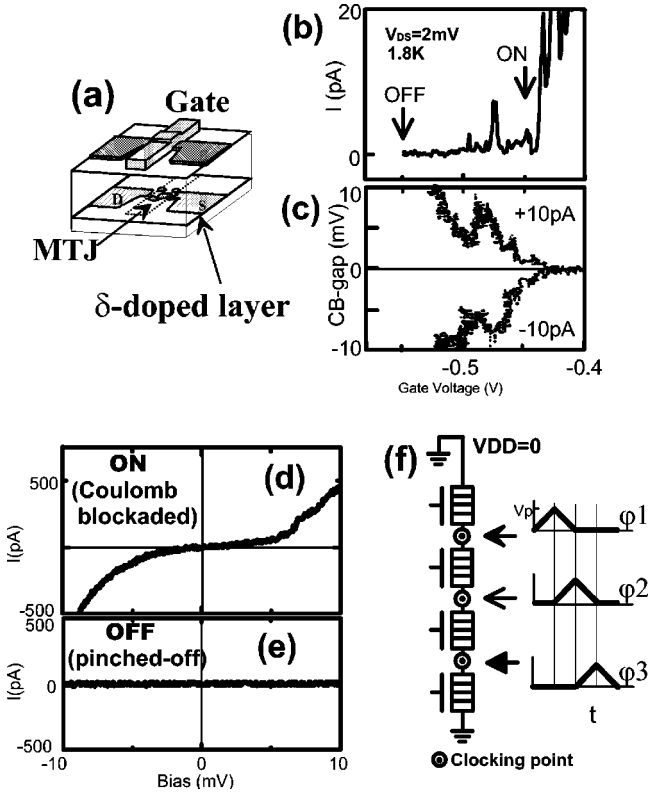

FIG. 2. (a) Schematic view of a CB transistor. Typical dc characteristics showing conductance oscillations (b) and CB gap oscillations (c) due to the CB effect in the one of the CB transistors in our integrated device. In the MTJ system, the periodic rhombic (diamond) CB gap, which can be observed in the SET with single island, cannot be observed because multiple size-varied islands contribute to the conduction. Typical current–voltage characteristics in the (d) ON and (e) OFF states. (f) Clocking scheme used to transmit an electron packet with phase delay ($\phi_1 - \phi_3$). V_p is the magnitude of the clocking pulse.

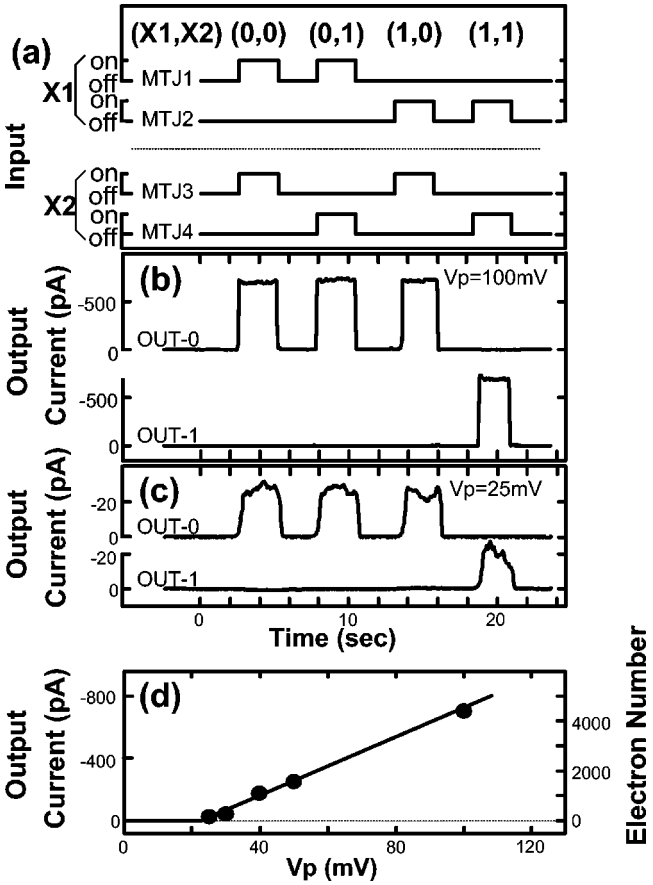

FIG. 3. (a) Input signals to the four gates (MTJ_1–MTJ_4). The typical voltage is −0.55 V for the pinch-off, and −0.45 V for the CB state. Output current for $V_p = 100$ mV (b) and 25 mV (c). The clocking frequency is 1 MHz. (d) Output current as a function of V_p at 1 MHz. The right axis shows the electron number transferred in each clocking modulation cycle from $I = \Delta n e f$. The solid line is guide to the eye.

eight CB transistors. An atomic-force microscope (AFM) image of the completed device is shown in Fig. 1(b). Each CB transistor consists of a gated narrow wire defined in the channel of δ-doped GaAs [Fig. 2(a)]. A negative voltage on the gate depletes the wire and squeezes the conducting channel. Impurity potential fluctuations cause the depleted wire to break up into a series of conducting islands separated by tunnel barriers, forming a multiple tunnel junction (MTJ).[12,13] The conducting islands are typically 10 nm in diameter, and the capacitance between islands is approximately 50 aF.[13] At our operating temperature of 1.8 K, transport through the MTJ becomes blockaded due to the influence of Coulomb charging [Figs. 2(b) and 2(c)]. In the blockaded state, the current–voltage characteristic appears as shown in Fig. 2(d). For substantial current to flow, the bias must surpass the CB gap.

Figure 1(c) shows an equivalent circuit for the device. There are three possible current pathways, each consisting of a series of four MTJs. We operate the MTJs in pumped mode under zero dc supply voltage ($V_{DD} = 0$).[3,9,10] This is shown explicitly in Fig. 2(f). Three phase-controlled pulses are applied to the clocking gates. The phase delay is set to be half of the pulse width. This places a bias difference sequentially across each transistor that temporarily exceeds the CB gap. Referring again to Fig. 1(c), the MTJs 1–4 can be placed in either an ON or OFF state, while the four unmarked MTJs are kept in an ON state. In the ON state [Fig 2(d)], the MTJ is in CB, so that a voltage pulse results in the passage of a packet consisting of a small number of electrons. In the OFF state [Fig 2(e)], a larger negative bias to the gate is applied to completely pinch off the conduction channel, and a voltage pulse has no effect. In our AND device, the first switching node X_1 is formed by the combined operation of MTJ_1 and MTJ_2 [Fig. 1(c)]. If MTJ_1 is ON, and MTJ_2 is OFF, the electron packet moves through the lefthand branch, towards OUT-0. This corresponds to an input of $X_1 = 0$. If MTJ_1 is OFF and MTJ_2 is ON, the electron packet moves through the righthand branch. This corresponds to an input $X_1 = 1$. Similarly, the MTJs 3 and 4 together form the second switching node X_2. The state $MTJ_3 = ON$, $MTJ_4 = OFF$ corresponds to the input $X_2 = 0$. This relation is summarized in Fig. 1(d). If both X_1 and X_2 are set to 1, a current is detected at the current amplifier OUT-1, otherwise, current is detected at OUT-0.

Figure 3 shows the results of measurements of the CB logic device at 1.8 K that demonstrate the AND function. As shown in Fig. 3(a), there are four possible inputs to X_1 and X_2, each corresponding to one combination of ON/OFF MTJs. The input signal is maintained for 2.4 sec. Figure 3(b) shows the output currents measured. There is a clear distinction between the high and the low states. For $V_p = 100$ mV at 1 MHz, the amplitude of the output current in the high state

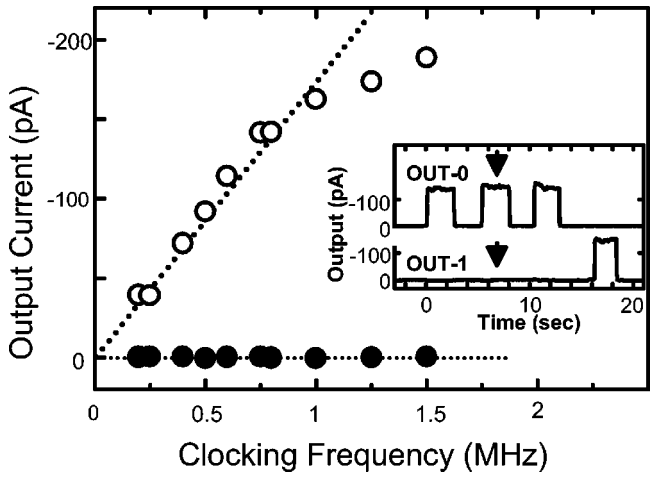

FIG. 4. Frequency dependence of the output current for $V_p = 40$ mV at OUT-0 (open circle) and OUT-1 (solid circle) measured at the point indicated by the arrows in the inset. The dotted lines are guides to the eye.

is -800 pA. The output current in the low state is less than the noise level (approximately 1 pA in our experiment). Note that the shape of the output pulses matches that of the input pulses and that overall, the output corresponds to that presented in the truth table of Fig. 1(d).

The amplitude of the output current decreases as V_p is reduced. For $V_p = 25$ mV, the logic function is still operational, but fluctuations in the signal are pronounced [Fig. 3(c)]. As shown in Fig. 3(d), the output current is linearly dependent on V_p, as long as V_p lies above the Coulomb gap. In Fig. 4, we plot the change in the output as a function of the clocking frequency (f), for $V_p = 40$ mV. The open circles show the current measured at OUT-0, and the filled circles show the current measured at OUT-1, for frequencies between 0.2 and 1.5 MHz. The amplitude of the pump current at OUT-1 is zero (within the noise level) and independent of f, while the amplitude at OUT-0 increases linearly with f up to 1 MHz.

The linear frequency dependence indicates that the pump current is generated by the sequential transfer of electron packets, each of which contains a fixed number of electrons. The number of electrons per packet is dependent on V_p, but independent of f. The pump current can be written as, $I = \Delta n e f$, where Δn is the number of electrons transferred in one clocking cycle, and e is the elementary charge. From the slope of our data, we estimate Δn to be 1080 for $V_p = 100$ mV. An estimation done for $V_p = 25$ mV shows that a minimum of 160 electrons per packet is needed to create a measurable logic function. In principle, the logic function is retained even if only one electron is transferred per cycle, but this is beyond the capabilities of our measurement circuitry. Above 1 MHz, the slope of the $I-f$ curve drops off. This is most likely caused by the large resistance capacitance (RC) delay of the MTJs.

Previously, the BDD logic architecture has been used in conjunction with MOS devices to create what is known as MOS pass-transistor logic circuits.[15] The MOS pass-transistor circuits have several advantages over conventional AND/OR combination circuits including higher packing density, lower power consumption and higher speed. The main disadvantage is that repeated connection of MOS switches results in a high series resistance and large supply voltage. Using the standard supply voltage, the number of switching nodes must be limited to four or five in series.

The multi-clocking scheme we employ in our CB logic device overcomes this problem, and in principle allows the series connection of a large number of switching nodes using no dc supply voltage. Even though the clocking method increases power consumption, the net power consumption should still decrease since the number of electrons per CB logic function is roughly 1% of that used in conventional devices. Since this system will only allow CB based combinatorial logic, any feedback functions, such as latch function, is difficult to be constructed without MOS devices. Also, improvements of the CB devices are needed: the operating temperature must be increased to at least 77 K,[16] and the RC delay of the MTJ should be reduced to raise the operation speed. This will require new strategies in CB device design.

This work was carried out under the management of FED as a part of the MITI R&D of Industrial Science and Technology Frontier Program (Quantum Functional Device project) supported by NEDO. The authors would like to thank M. Kirihara, K. Katayama, H. Mizuta, H.-O. Müller, and D. G. Hasko for useful discussions.

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