Emission lifetime of polarizable charge stored in nano-crystalline Si based single-electron memory

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The lifetime of the emission of a single electron stored in a nanocrystalline Si (nc-Si) dot has been studied in order to understand the physical processes for memory applications. A small active area field effect transistor channel (50×25 nm) is defined by electron-beam lithography on a thin (20 nm) silicon-on-insulator channel and allows for the electrical isolation of a single nc-Si dot. Remote plasma enhanced chemical vapor deposition is used to form 8 ± 1 nm diameter nc-Si dots in the gas phase from a pulsed SiH_4 source. Electrons stored in a dot results in an observed discrete threshold shift of 90 mV. Analysis of lifetime as a function of applied potential and temperature show the dot to be an acceptor site with nearly Poisson time distributions. An observed $1/T^2$ dependence of lifetime is consistent with a direct tunneling process, and interface states are not the dominant mechanism for electron storage in this device structure. Median emission lifetimes as a function of applied gate bias are readily modeled by the polarizability of an electron in a delocalized bound state over the entire semiconducting dot. © *2001 American Institute of Physics.*
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I. INTRODUCTION

Memory sensitive to the charge of a single electron has the possibility to drastically improve device characteristics in terms of high density, low power, fast write/erase, and long retention time. With current scaling trends in metal–oxide–semiconductor field-effect transistors (MOSFET) there is the inevitable need to understand and optimize devices that operate with only a statistically small number of electrons whose transport is mesoscopic. Si based nanoscale devices are strong contenders due to the existing Si process infrastructure as well as the nearly perfect interface between SiO_2 dielectric and Si. The latter advantage is paramount to success, since single electronic devices are inherently sensitive to local and background charged defects. Recent advances in crystal growth result in the formation of 5–10 nm diameter nc-Si dots without the need for complex lithography.[1] With crystals of these dimensions the Coulomb charging energy is significant and would be the basis for single electron transistors as well as the self-limited charging of floating gate memory nodes.

Several groups have demonstrated single electron memory effects in Si systems. Examples include a charge stored in nanocrystalline Si dots (nc-Si) above a large area FET channel,[2] a charge stored in a single poly-Si dot over a narrow silicon-on-insulator (SOI) channel,[3–5] and memory devices based on charge through complex percolation paths of several nm thick SOI.[6] Generally there is a significant trade-off between short write/erase time and long memory retention time, which is determined mainly by the tunnel oxide thickness in devices that use nc-Si dots as a floating gate storage node. The write time is reported to be many orders of magnitude faster than retention time,[2] which is not expected if both the write and erase process are due to direct tunneling. One possible explanation for the long retention time is that stored electrons are trapped in interface states on the Si nanocrystals. This effect of interface states on nc-Si based memory has been shown to be important after the H passivation of interface states are removed by annealing.[7] However, the role of interface states in initial devices is not known and is likely dependent on processing methods. Large area transistor studies[8] show that there are two distinct lifetimes, which could be interpreted as fast direct tunneling emission followed by slower trap related emission. However, this analysis is complicated by the effect of the resultant electric field from a stored charge that accelerates the initial discharge process. Another large area transistor study[9] shows there to be a small temperature dependence on a dynamic charging suggesting that interface states are not critical, rather a steady state charge is reached when tunneling current from floating dot to gate equals that of channel to floating dot. However, in this study, operation is under high electric field where Fowler–Nordheim tunneling occurs, which would similarly show tunneling from electrons in relatively deep traps. Similar memory devices have been made for nc-Si grown on a Si_3N_4 tunnel barrier.[9,10] The advantage of a Si_3N_4 system is a higher aerial density of nc-Si grown by chemical vapor deposition (CVD) as well as a reduced tunnel barrier height. The nitride system is commonly known to have a higher density of localized defect sites but discharge properties are roughly similar to the Si/SiO_2 system suggesting defect states are not critical. Photoluminescence studies of nc-Si dots imbedded in an oxide matrix[11] or from pulsed laser deposition[12] tend to show a light emission in visible energies which can be attributed to an increase in band gap from the quantum confinement of reduced dot size or carrier

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recombination in characteristic oxide defects. Although currently the subject of continued investigation, it is likely due to a coupling of the two effects.[13] This would indirectly suggest that interface states of the nc-Si dot would play a significant role in charge retention. Another factor which suggests that traps in the nc-Si/SiO_2 interface is that there are many crystal step edges from multiple faces that would likely be a source of dangling Si bonds.

To be able to distinguish if charge is delocalized over the entire dot or trapped in a localized defect on the dot requires the study of a single dot. This is because a distribution of dot sizes and complex electron percolation path in a transistor channel would make analysis of multidot systems impossible. Reports of single electron memory using a single poly Si dot defined by twice aligned electron-beam lithography focused on the self-limited charging of memory and no lifetime studies are reported.[3] However, it is reasonable to expect a significant role for interface states due to the process conditions to form a poly-Si dot.

Remote plasma enhanced chemical vapor deposition (RPECVD) using a pulsed source reactants readily forms single crystal nc-Si dots (nominal 8 ± 1 diameter) in a gas phase process.[1] The advantage of this process over other CVD processes is that spherical dots with good passivation and small size dispersion are formed without the codeposition of amorphous-Si, which can act as charged defect sites. Although the exact location of deposited nc-Si is not controlled, by making a channel with a small active area, we can statistically isolate a device where a single nc-Si dot will determine the memory state. Presented here are the results of memory lifetime analysis as a function of temperature and applied gate bias, which show that interface traps do not dominate memory retention time.

II. EXPERIMENTAL DETAILS

The schematic of the field effect transistor (FET) with nc-Si floating gate nodes is shown in Fig. 1(a). The device fabrication process begins with the dry-oxidation thinning of the separation-by-implanted-oxygen (SIMOX) silicon layer to 25 nm and partial HF chemical etching of the top oxide layer. The buried oxide thickness is 400 nm. The entire wafer is lightly doped by phosphorus implanted to 4×10^{17} cm^{-3}, diffusion annealed at 900 °C for 30 min, then top oxide removed by HF etch. Patterns [Fig. 1(b)] for narrow Si channels (25 nm wide and 50 mm long) are written by an electron beam (EB) lithography apparatus [JEOL JBX5(FE)]. The EB process uses an RD2000N negative resist, which has high sensitivity to electron exposure and high resistance to subsequent dry etching.[14] The active area of the device results from the proportionately higher resistance due to the smaller cross sectional area of the narrow channel. Series resistance outside of the gate area is reduced by using 50 μm wide leads. Next, electron cyclotron resonance reactive ion etching (ECR-RIE) is used to transfer the resist pattern to the SOI layer, using CF_4 as a reactive gas. To remove plasma damage and residual fluoride on SOI by the RIE process, 3 to 4 nm of the thermal oxide is grown by dry oxidation at 800 °C for 20 min and then removed in diluted HF (0.75%)

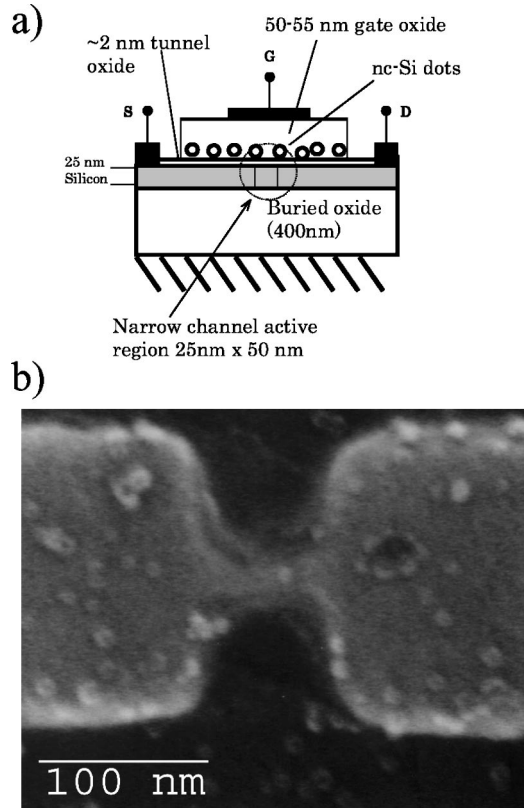

FIG. 1. (a) Schematic of single electron memory device isolating a single nc-Si dot as a floating gate memory node. (b) Planar scanning electron microscopy view of a representative memory device after nc-Si dot deposition showing a single nc-Si dot near the center of the narrow channel active region. The dark region outside of pattern is buried oxide.

solution. Chemical oxidation by H_2SO_4/H_2O_2 subsequently forms a 2 nm oxide tunnel barrier. Next nc-Si dots of nominal 8 ± 1 nm diameter are deposited by RPECVD for a density of 1×10^{11} cm^2. This gives 1 to 2 dots in the active area. A 50 nm thick gate oxide is deposited by tetra-isocyanate silane (TICS) PECVD at 300 °C. The quality of this PECVD oxide is similar to that of thermal oxide after a high temperature anneal.[15] The contact pad area was heavily doped (5×10^{19} cm^{-3}) by P implant, followed by an N_2 anneal at 1000 °C for 1 h. The anneal serves to improve gate oxide quality and to activate dopants. Finally, contact pads and gate electrodes are formed by the Al lift-off technique. The memory device is mounted on a probe station connected to a cryostat cooler, which permits temperature as low as 20 K. A semiconductor parameter analyzer (HP4156B) and pulse generator (HPB1104A) with automated collection software is used for electrical measurement.

III. RESULTS

The basis of single electron memory is to have a discrete shift in threshold voltage (V_{th}) from the screening effect of charge stored in the dot above the FET channel. Figure 2 shows a representative observed shift in V_{th} from electron storage and emission from a nc-Si dot. The observed shift in V_{th} of 90 mV can be expected for a single charge over a 25 nm wide channel and a gate oxide thickness of 50 nm. Notable is the discrete step in conduction at a constant gate bias

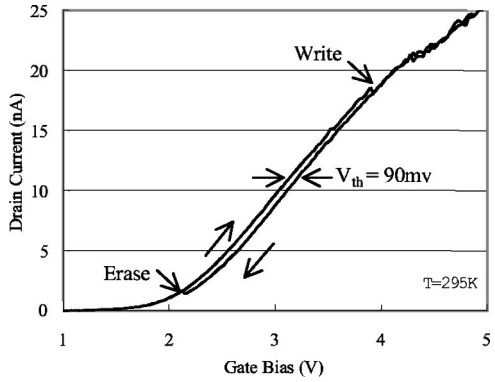

FIG. 2. Observed threshold shift for a small area FET channel with nc-Si floating gate memory.

after a writing pulse in Fig. 3. A stepwise increase in conduction clearly shows the discrete emission of an electron from the nc-Si dot. It should be noted that the data shown in Fig. 3 is a representative example of memory lifetime and that there was significant distribution of lifetimes for other pulses under the same conditions. Thus to have an accurate measure of the lifetime distribution it is necessary to measure lifetime using at least several hundred cycles. To study erase time in a statistical manner, the applied pulse sequence is shown in the inset of Fig. 4. The erase time is the cumulative time under erase bias pulses until there is a step increase in conductance. Figure 4 shows a histogram of memory lifetimes after 400 write/erase cycles as a function of applied erase bias. As expected the dots acts as an electron acceptor site, with reduced lifetime as more negative gate bias is applied. However, this effect is relatively small indicating that the electron is not likely stores in a trap since this would be sensitive to Fermi level location relative to trap level. Another important aspect of Fig. 4 is that the distribution of lifetime is quite broad with the mean value being nearly equal to the standard deviation. A Poisson distribution is expected for a process with high attempt frequency but low probability of emission. The median lifetime as a function of gate bias is shown in Fig. 5. In this figure the median emission lifetimes for the negative bias data is from the distribution shown in Fig. 4 with pulsed erase/read measurement. At positive bias, emission lifetimes are measured directly at the given reading voltage with a step in conduction after a write

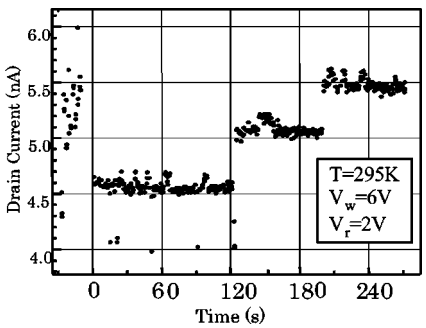

FIG. 3. Time dependence of channel current after writing process. Stepwise increase in current is due to electron emission from a nc-Si dot in the active region.

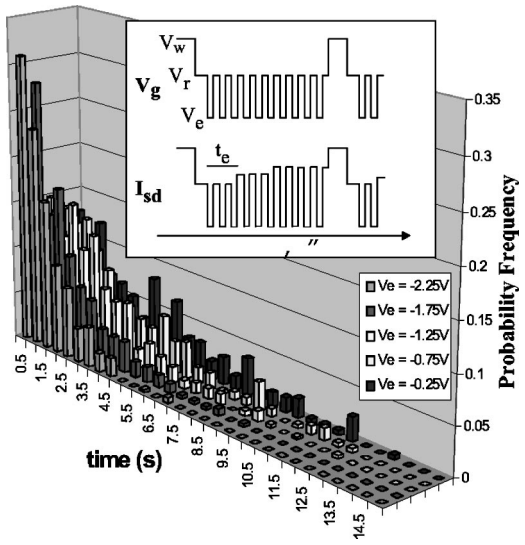

FIG. 4. Distribution of memory lifetimes as a function of applied erase bias V_e at 295 K (front series is at $V_e = -2.25$ V). Inset shows pulse sequence. Writing voltage $V_w = 6$ V, reading voltage $V_r = 0.25$ V, 0.1 s read, 0.1 s erase pulse time. 400 cycles at each V_e.

pulse at the given reading voltage as is seen in Fig. 3. Most notable is the rather small dependence of lifetime on bias over a large voltage range and different slopes for positive and negative bias. The temperature dependence of lifetime would show if a thermionic emission process is present. Figure 6 shows that there is a very small temperature dependence on lifetime and an absence of an activation energy. If interface states act as electron traps then an activation energy from 50 to 200 mV would be observed.[16] The temperature dependence of lifetime is seem to be proportional to $1/T^2$, which is consistent with a direct tunneling process which depends on the density of states in the channel to tunnel into $(T^{3/2})$ times thermal velocity $(T^{1/2})$ of the stored electron.

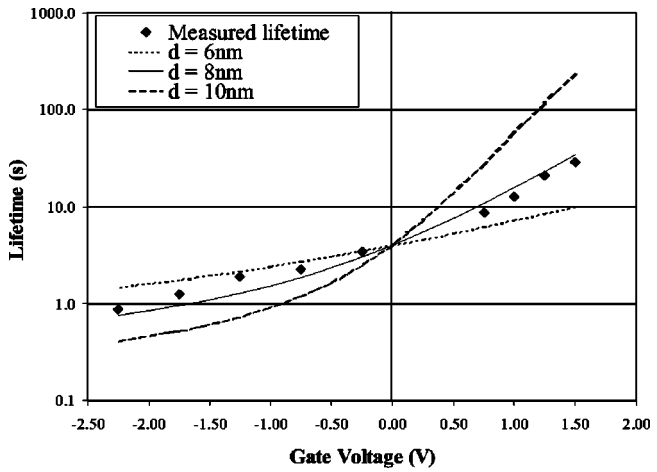

FIG. 5. Observed median lifetime (solid points) of a nc-Si memory device as a function of applied gate bias. Shown curves are calculated from a polarizable Schrodinger equation for a one-dimensional confined potential well at the given nc-Si dot diameter. Each lifetime curve for a given dot diameter is normalized at 0 V gate by changing tunnel oxide barrier.

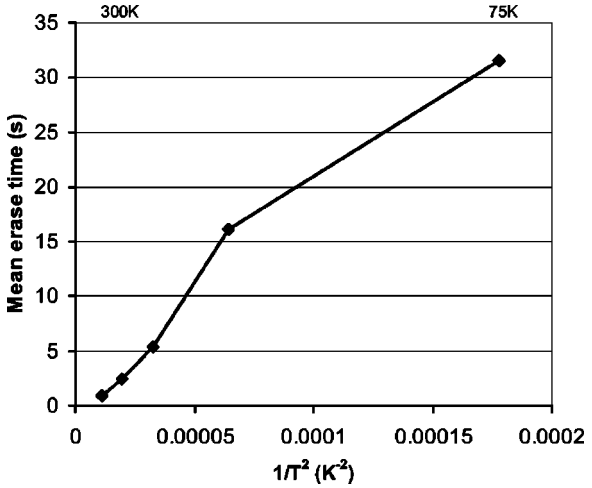

FIG. 6. Temperature dependence of memory erase time at $V_e = -2.25$ V. Shown is mean lifetime after 250 erase cycles as shown in Fig. 4.

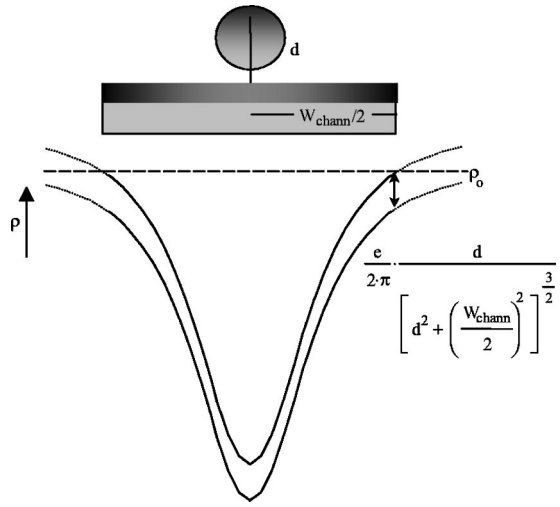

FIG. 7. Schematic of surface electron density on a SOI channel under a nc-Si dot as calculated from the simple image charge model. The dashed line indicates electron density (ρ_0) on top of the inversion channel before addidtion of screening charge into the nc-Si dot. The small vertical line represents the amount of charge required to bring ρ to the edge of the channel where maximum conduction would be.

IV. DISCUSSION

The observed discrete shifts in channel conductance and shift in threshold voltage are qualitatively consistent with a single electron process of memory storage. In particular it is important to qualitatively model the threshold shift and lifetime dependence with temperature and gate bias to determine whether the electron is delocalized over the entire nc-Si dot. With an accurate model of the physical process further discussion can be made about optimizing memory design to take advantage of single electron storage.

A. Device geometry and observed threshold shift

The basis of the device being sensitive to a single charge is simply reducing the area of the channel so that statistically one nc-Si will be present. With a larger channel area the shift from a single dot would be expected to be less. In previous studies of a single poly-Si dot over a narrow Si channel threshold shifts are well approximated by $e/(C_{gd}+C_{gc})$ where the C_{gd} is the gate to dot capacitance and G_{gc} is gate to channel capacitance.[3,4] Capacitances are estimated by the infinite parallel plate method. However, the exact value of C_{gd} is difficult to estimate because of an unknown length for which the charge in the dot screens charge in the channel. Guo *et al.*[3] found that the Debye screening length of 70 nm worked well while Nakajima *et al.*[4] found that the entire channel length under the control gate of 200 nm appropriate to calculate C_{gc}. The difficulty of using the Debye screening length as a basis for the C_{gc} area is that in moderate inversion conditions the screening length is reduced from 70 to 1 to 2 nm but there is no change in V_{th} shift as would be expected for a reduced C_{gc}. In our present device using the entire device area of 50×25 nm plus an equal area of side wall capacitance gives a C_{gc} of 1.7 aF and C_{gd} of 0.04 aF for an 8 nm diameter dot. This results in a V_{th} shift of 90 mV, which is very close to the experimentally observed value. The use of lithography to directly limit the channel length in the narrowest region appears to limit the length of the stray channel capacitance that detrimentally reduces V_{th} shift. However, it becomes an interesting question as to why the screening charge should affect such a large area of the channel. As a charge approaches a conducting plane (a valid approximation of charge in a nc-Si dot over a channel in deep to moderate inversion) one can use the image charge equation to solve the reduction in surface density of screened conducting electrons. This is diagramed in Fig. 7. To return the electron density for the area directly under the dot to the previous level (without screening charge) would require a very large applied gate bias ΔV_0 as in Eq. (1) where t_{gox} is gate oxide thickness and A is an arbitrary area for the active device.

$$\Delta V_0 = \frac{e \cdot t_{gox}}{\varepsilon_{ox} \cdot A}, \tag{1}$$

$$\Delta V_{th} = \frac{\Delta V_0}{\frac{e}{A}} \frac{e \cdot d}{2\pi\left[d^2 + \left(\frac{W_{chann}}{2}\right)^2\right]^{3/2}} = \frac{t_{gox} \cdot e}{\varepsilon_{ox} \cdot 2\pi} \frac{d}{\left[d^2 + \left(\frac{W_{chann}}{2}\right)^2\right]^{3/2}}. \tag{2}$$

With small A, on the dimension of nc-Si dot, there would be a drastic increase in the electron density for the channel region away from the dot and would strongly overestimate the threshold shift. In this simple approximation we take into account the width of the channel (where the minima in screening would be) and calculate the required applied gate bias to bring the electron density at the edge back to the density before the addition of screening charge. This is given in Eq. (2) where d is dot diameter and W_{chann} is channel width. The arbitrary area of active device, A, is algebraically cancelled out. For our device, dimensions of an 8 nm dot with a 25 nm channel with a V_{th} shift of 90 mV are calculated consistent with experimental observation. Using this same model would predict a shift of 50 mV ($d=4$ nm,

$W_{chann}=27$ nm, $t_{gox}=40$ nm) for Guo *et al.*'s single poly-Si dot over a narrow Si channel compared to an observed V_{th} shift of 55 mV. In Nakajima *et al.*'s similar device this model predicts a V_{th} shift of 130 mV ($d=18$ nm, $W_{chann}=40$ nm, $t_{gox}=200$ nm) to their observed value of 100 mV, which would be within the uncertainty of device dimensions and electrical measurements. For Welser *et al.*'s[5] similar device it is difficult to experimentally ascertain the single electron threshold shift due to the relatively large size of the poly-Si dot. Iannaccone *et al.* calculated a population of about 60 electrons in the dot for an experimentally observed V_{th} shift of 0.75 V or 12 mV/e^-.[17] Using the image charge approximation described here ($d=10$ nm, $W_{chann}=40$ nm, $t_{gox}=20$ nm) results in a V_{th} shift of 12 mV/electron. In this case the simple parallel plate capacitance model gives a V_{th} shift of 21 mV/electron ($C_{gc}=4.6$ aF, $C_{gd}=3.1$ aF). Another aspect of the image charge model is that the length of screening over the channel is a function of dot height above the channel and extends for a considerable distance. For instance an electron in an 8 nm diameter dot would have an image charge of $-0.7e$ along a 80 nm long channel surface that is 30 nm wide. This would explain why this model is in rough agreement with the simple capacitance model using a large channel length as well as why the drastic reduction of Debye length while channel is inverted does not effect the observed V_{th} shift.

B. Emission lifetime dependence on temperature and gate bias

One challenge with single electron devices is the inherent sensitivity to charge trapped in localized interfacial or bulk oxide defects. Since a defect charge in the active area would have a similar shift in V_{th} as would a charge stored in a nc-Si dot over the channel, it is important to look closely at the temperature and gate bias dependence of lifetime to distinguish the two mechanisms. In the case of deep near-interfacial traps, the lifetime of the individual defect site has been well characterized by looking at a random telegraph signal (RTS) of the channel current for small area FET transistors.[18–20] In particular the emission lifetime (τ) for a RTS signal is strongly temperature activated and found to have a linear relationship between $\ln(\tau^* T^2)$ and $1/T$. The T^2 term is a result of the product of thermal velocity and density of states as commonly used to describe emission processes in semiconductors. For an observed RTS from trap sites activation energies on the order of 50–200 mV are seen.[16] A linear dependence with $1/T^2$ was observed, which is consistent with a direct tunneling process. If a defect were present on the nc-Si/SiO_2 interface, instead of on the channel/SiO_2 interface, there would also be a strong temperature dependence that was not observed. The gate bias dependence of defect related RTS lifetime is also markedly different than what is observed in this nc-Si system. In the RTS case a logarithmic lifetime dependence is found with gate bias as the alignment between Fermi level and trap level changes,[18] while in the nc-Si system we observe a weak dependence of lifetime with gate bias. Thus we are able to infer that the observed electron emission in the nc-Si memory is not from a defect site on the SOI channel/SiO_2 interface nor the nc-Si/SiO_2 interface. Figure 8 shows a schematic of the energy diagram for a Si dot with interface traps at positive and negative bias. The temperature dependence of emission time eliminates a thermionic route of exciting trapped electron in to the conduction band of the dot. At positive bias the trap is below Fermi level and hence filled eliminating a nc-Si interface trap to channel interface trap tunneling mechanism. Also there is a small probability that a trap on the channel is both spatially and energetically aligned with a trap on the dot interface making a trap-to-trap emission unlikely at high bias. In a negative bias dot-trap to channel-trap tunneling mechanism there would be a strong gate bias dependence on trap energy level alignment that is not observed. Thus the observed lifetimes are consistent with the electron being delocalized over the entire nc-Si dot.

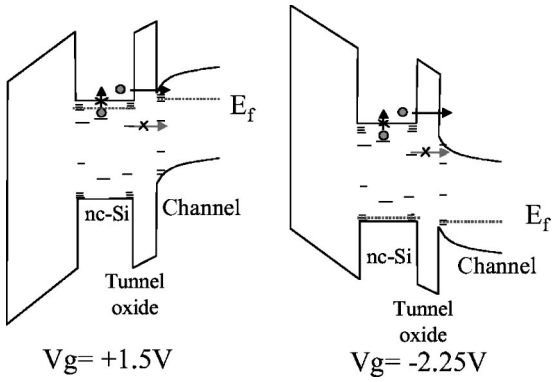

FIG. 8. Energy diagram of trap states for the electron emission process from a nc-Si dot.

C. Memory lifetime model based on the polarizability of a delocalized electron

Since the stored electron behaves as if it were delocalized, it is an interesting question as to whether the electron is in a bound state for the entire dot. Since we are applying gate bias from a top gate we can approximate Schrodinger's equation to the one-dimensional charge in a potential well system. To explain the lifetime as a function of applied gate bias, an important concept is that the electron will be attracted to the top of the dot with positive bias thus reducing the tunnel current from the bottom of the dot into the channel. Shifts in the electron probability (Ψ^2) are shown in Fig. 9. In order to calculate polarization shifts one must first know the potential drop across the dot by accounting for the difference between dielectric constants for Si(11.9) and SiO_2(3.9). However, the dot size is so small that the parallel plate capacitor treatment is a poor approximation, and Poisson's equation must be solved in three dimensions. The potential profile across the three-dimensional dot was calculated numerically[21] for dielectric dots without free carriers as a function of dot diameter. The empirical fit of the dielectric factor (df) for the potential drop across the dot is shown in Eq. (3) where d is dot diameter, t_{gox} is gate oxide thickness, and t_{tox} is tunnel oxide thickness. The potential drop across the dot is in-

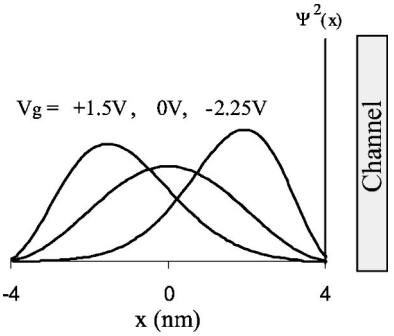

FIG. 9. Calculated one-dimensional electron wave function in an 8 nm diameter nc-Si dot under applied gate bias from the left side.

creased by a factor of 1.5 and 1.7 times the infinite parallel plate model [first term of Eq. (3)] as dot size is decreased from 12 to 4 nm.

$$df=\frac{\dfrac{d}{11.9}}{\left(\dfrac{t_{\text{gox}}}{3.9}+\dfrac{d}{11.9}+\dfrac{t_{\text{tox}}}{3.9}\right)}\cdot(1.806-0.0241\cdot d). \tag{3}$$

Schrodinger's equation under an applied electric field, F [Eq. (4)], is then solved. The equation is first reduced to the dimensionless form in Eqs. (5) and (6), where energy E is found iteratively using the Runge–Kutta method after an initial guess from perturbation theory. m_{eff} in Si of $0.32m_e$ is used. The term d_{eff} is the effective diameter of the nc-Si dot for an infinite potential (for a given $d=8$ nm, $d_{\text{eff}}=8.386$ nm). To calculate d_{eff} the zero field wave-function solution for Ψ is analytically found[22] for a dot with diameter d with a barrier height of 3.2 eV.[24] π/k of the resulting wave function is d_{eff}. Thus at $x=d/2$, the wave function (Ψ) of an infinite well with diameter d_{eff} has the same value as a 3.2 eV well with diameter d. By using d_{eff} the high field solution of Eq. (5) is readily solved due to the simple boundary condition of $\Psi\,(d_{\text{eff}}/2)=0$ with negligible error at $x=d/2$. For calculating tunneling probability of the electron out of the bottom of the dot, $\Psi(d/2)^2$ is used.

$$\frac{-\hbar}{2m}\frac{d^2\Psi(x)}{dx^2}+x\cdot e\cdot F\cdot\Psi(x)=E\cdot\Psi(x), \tag{4}$$

$$\frac{d^2}{dx^2}\Psi(x)+\Psi(x)\cdot x\cdot\left[-\left(e\cdot V_g\cdot\frac{d_{\text{eff}}}{d}\cdot\frac{df}{\pi\varepsilon_1}\right)\right]=\frac{E}{\varepsilon_1}\cdot\Psi(x), \tag{5}$$

$$\varepsilon_1=\frac{\hbar^2\pi^2}{2m_{\text{eff}}d_{\text{eff}}^2}. \tag{6}$$

The memory lifetime is the inverse of tunneling current $(1/J_t)$ for an electron at the bottom, or channel side of the dot. The tunnel current is given by Eq. (7).

$$J_t=\frac{\left(\dfrac{3k_bT}{m_{\text{eff}}}\right)^{1/2}}{2d}N_cT^{3/2}\cdot\left[\Psi\left(\frac{d}{2}\right)\right]^2\cdot\exp\left[-2\left(\frac{2e\cdot m_{\text{effox}}\phi_b}{\hbar^2}\right)^{1/2}t_{\text{tox}}\right]. \tag{7}$$

The first term is the thermal velocity (v_{th}) divided by twice the dot diameter, which is the escape attempt frequency. The second term is the normalized density of states N_c (300 K) in the Si channel for the electron to tunnel into. The third term is the electron density at the bottom of the dot $\Psi(d/2)^2$, and the final term is the tunneling probability where t_{tox} is the tunnel oxide barrier thickness, $m_{\text{effox}}=0.42m_e$ is the effective mass of tunneling through an oxide barrier,[23] and Φ_b is the oxide tunnel barrier of 3.2 eV.[24] Figure 5 shows the calculated lifetimes as a function of gate bias for three different nc-Si dot diameters. The fits to the model shown in Fig. 5 use dot size and tunnel oxide thickness as adjustable parameters, as they cannot be precisely determined experimentally. Each fit was normalized to the lifetime at $V_{\text{gate}}=0$ by changing tunnel barrier thickness (2.58, 2.50, and 2.45 nm for $d=6$, 8, and 10 nm, respectively). The various slopes are a result of the larger dot size being more easily polarized. A dot size of 8 nm best represents the observed data and is consistent with the physical diameter of deposited dots. Importantly the proposed model accounts for the relatively small gate bias dependence on memory lifetime and predicts two different slopes for positive and negative gate bias. However, the self-limiting Coulomb charging as well as threshold shift V_{th} would then be significantly reduced, thus impairing overall device performance. Lifetime can be improved by increasing the tunnel oxide thickness but this would also increase write and erase time in a similar fashion. For DRAM applications (refreshed memory), a delocalized electron over the entire dot gives a predictable memory system with a time scale that can be readily adjusted by tunnel oxide thickness. For long term retention in flash memory applications, the direct tunneling mechanism means that write/erase and retention times cannot differ by the required ten orders of magnitude.

To improve retention time while not increasing write/erase times it is possible to take advantage of shallow interfacial traps on the nc-Si interface. These can be intentionally added by forming a nitride on the nc-Si dot before depositing SiO_2 gate dielectric. During writing, the electron density would be polarized to the top of the dot and localized in a defect trap at the top. This charge would be unable to directly tunnel into the channel due to the long tunneling distance across the nc-Si dot and results in long retention times. With applied erase gate bias, emission can be attained by two mechanisms. The first is thermionic emission from a trap at the top of the dot into a delocalized state over the entire dot followed by localization in a trap at the bottom of the dot. A shallow trap's energy level will align with the conduction band of the channel at relatively low erase bias and directly tunnel into the channel. The second mechanism would involve the hopping of electron from trap sites on the outside of the dot to the channel side during erase bias, from which

it could tunnel into the channel. If defects are spatially dense then conduction on the outside of the dot can be expected without benefit to lifetime. Also if the trap energy is too deep, a high erase bias will be required or long erase times would be expected due to slow thermionic emission. Thus control of trap level and area density on the nc-Si dot is required and Si_3N_4 is a promising candidate with relatively shallow defect sites and conduction by hopping mechanism.

V. CONCLUSIONS

Reduction of a FET channel area on an SOI substrate by lithography can make a memory device sensitive to the charge of a single electron stored in a nc-Si floating gate. These nc-Si dots formed by RPECVD with subsequent thermal annealing are found to have low interfacial defect density. In fact the lifetime of the memory devices is consistent with an electron delocalized over the entire nc-Si dot without significant influence of deep interfacial traps. Similar behavior could be expected from other devices if processing insures a good Si/SiO_2 interface with nc-Si. By using a model that accounts for the ability to localize charge at the top of the dot away from channel, the gate bias affect on lifetime is predicted. It is found that a polarizable wave function of an electron in a bound state of the nc-Si dot with direct tunneling into the channel is consistent with observed lifetime data.

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