

Performance of the Raith 150 electron-beam lithography system

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The performance of a Raith 150 electron-beam lithography system is reported. The system's resolution, stability, intrafield distortion, stitching, and overlay performance are evaluated. Patterning at low- and high-acceleration voltages is compared. The system was used to pattern sub-20 nm features, and the largest intrafield distortion for a 100 μm field was measured to be 15 nm. Pattern-placement accuracy below 35 nm, mean plus twice the standard deviation, was demonstrated. © 2001 American Vacuum Society. [DOI: 10.1116/1.1414018]

I. INTRODUCTION

Recently, a new electron-beam lithography tool, the Raith 150 Turnkey system,¹ has become commercially available for research and small business applications. The core of the system is a LEO 1500 series scanning electron microscope,² which has been converted for large-area pattern generation with the addition of necessary hardware, software, an increased chamber size, and a laser-interferometer-controlled stage. Because of its thermal-field-emission source and Gemini² column, the tool promises high-resolution lithography.

Several experiments have been carried out to evaluate the Raith 150's resolution, stability, intrafield distortion, stitching, and overlay performance. Also, patterning was tested at low- and high-acceleration voltages. Above an acceleration voltage of 20 kV, feature sizes as small as 17 nm were patterned, and the field-stitching performance was better than 25 nm, mean plus standard deviation. At 10 kV, the overlay accuracy at the field center was better than 30 nm, mean plus standard deviation. Details of the experiments are reported in the following sections.

The Raith 150 system was purchased as part of a research program at MIT to reduce the pattern-placement accuracy to the 1 nm level via spatial-phase locking (SPL).³ The system has several desirable features for its adaptation to spatial-phase locking. Only non-SPL results will be reported in this article, and soon the authors hope to report its improved placement performance separately.

II. HIGH-RESOLUTION PATTERNING AT LOW- AND HIGH-ACCELERATION VOLTAGES

The Gemini column's imaging resolution, measured at the factory and on site using an edge-sharpness method, is found to be less than 4 nm over the tool's acceleration-voltage range, and suggests a sub-10-nm-diam beam. Uncommon to most electron-beam-lithography systems, the Raith 150 offers flexibility in beam-acceleration voltage (from 200 V to 30 kV), and focal length or working distance (20 mm to <1 mm). To minimize intrafield distortion (see Sec. IV), the

working distance was maintained near 6.5 mm. High-resolution patterning was tested at several acceleration voltages from 1.5 to 30 kV.

The short electron range at low acceleration voltage, <150 nm in polymethyl(methacrylate) PMMA⁴ at 2 kV, requires the use of thin resists.^{5,6} Two resist stacks, shown in Fig. 1, were used in our experiments. One stack [see Fig. 1(a)] was a 50-nm-thick, single layer of PMMA. A 950 K-molecular-weight PMMA, 1% solution in chlorobenzene, was spun onto a bulk silicon substrate, and then baked for 1 h at 140 °C. A second trilayer stack [see Fig. 1(b)] was used for more robust pattern transfer, i.e., deeper etches or thicker deposition. This stack consisted of a 120-nm-thick bottom polymer layer, XHRi-11 from Brewer Scientific chosen for convenience, a 30-nm-thick oxide interlayer, and the same 50-nm-thick PMMA layer. After exposure, the resist development was done at 21 °C in methyl-iso-butyl-ketone, 33% dilution in isopropyl alcohol, for 45 s.

The cleanest, highest-resolution patterns were obtained with the single-layer resist, and example features are shown in Fig. 2. A dose matrix was written, and the patterns were transferred to the substrate via a liftoff process. Two metal layers, 5 nm of chrome and 15 nm of gold, were deposited in sequence with an e-beam evaporator. The "star" patterns show that the e-beam was well stigmated for the exposures. The finest features reported are those for which the metal lines were unbroken over their entire 5 μm length.

The 46 nm linewidth shown in Fig. 2(a) was written with an acceleration voltage of 1.5 kV and a linear dose of 33 pC/cm, and the 19 nm linewidth in Fig. 2(b) was patterned at 30 kV and a dose of 900 pC/cm. The uncertainty of the linewidth measurement is ± 2 nm. The finest linewidth produced was 17 ± 2 nm, and was part of a pad-and-gate structure. The more substantial line-edge roughness for the low-voltage exposure is believed to be due to the resist profile, positive sloping, or feet which degrade the liftoff. Fine lines were also produced with the trilayer stack, and transferred deep into a substrate. In one experiment, 47-nm-wide trenches were etched 214 nm deep into an oxide substrate, using the trilayer stack, liftoff processing, and reactive-ion etching. An acceleration voltage of 20 kV was used for this trilayer experiment.

Although the patterning resolution was not as good at low

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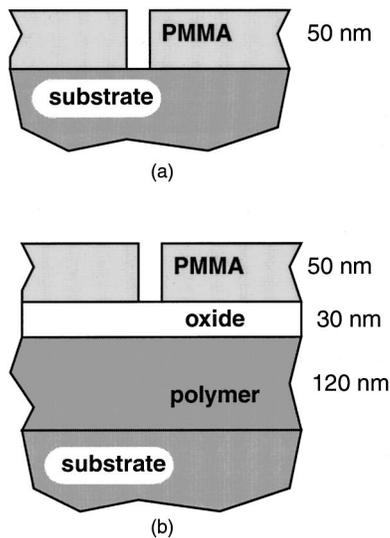


FIG. 1. Low- and high-voltage resist stacks. (a) Single-layer resist stack for thin additive-pattern transfer or shallow etches. (b) Trilayer resist stack for more robust pattern transfer.

voltage as at high voltage, there are two advantages to writing at low-acceleration voltages: reduced proximity effect and reduced exposure time. Our findings on proximity effect were consistent with those reported previously in similar work.⁶ However, in our experiment the exposure dose required at 2 kV was about 1/10 the value required at 20 kV, a difference not noted in the earlier work.

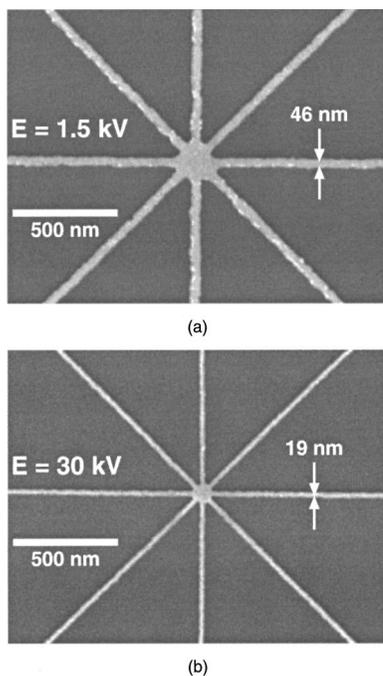


FIG. 2. High-resolution metal-on-silicon patterns: (a) 46-nm-wide isolated lines patterned at 1.5 kV; and (b) 19-nm-wide isolated lines patterned at 30 kV. The star pattern indicates a well-stigmated beam.

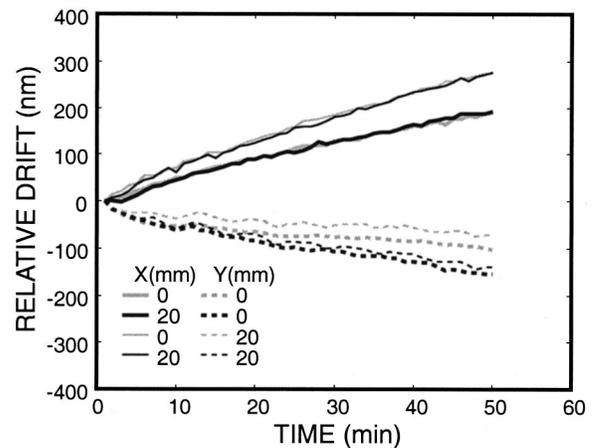


FIG. 3. Plots of the electron-beam drift over time, relative to four locations on the sample. The positional drift was less than 6 nm/min, and the rotational drift was less than 0.1 μ rad/min.

III. SYSTEM STABILITY

The drift of the electron beam, with-respect to the laser-interferometer stage, was carefully measured before attempting field-stitching and overlay measurements. There are several potential causes for beam drift which may vary over time: thermal effects in the column or the stage, charging in the column, chamber, or on the sample itself. The drift measurements were carried out with a conductive sample, and repeated on several different days.

At least 3 h prior to beginning drift measurements, a patterned sample was placed on the substrate chuck and in the vacuum chamber. This allowed thermal equilibration of the chuck and sample to conditions inside the chamber. The patterns on the bulk silicon sample were four global-registration marks: gold bars, 100 nm wide by 2 μ m long, in the shape of a right angle. This permitted X and Y registration at four locations on the substrate. The four marks were separated by 20 mm in a square array. The use of four marks enabled the determination of drift values for position and rotation of the substrate with respect to the electron beam, as well as thermal expansion of the substrate.

The four marks on the substrate were scanned sequentially at 1 min intervals for about 1 h. The marks were always scanned at the field center to minimize intrafield-distortion and field-calibration errors. An example of their positional drift is graphed in Fig. 3. From this and similar data collected on different days, the positional drift was found to be less than 6 nm/min. The thermal stability, measured near the column outside the chamber, was typically better than 0.3 $^{\circ}$ C during the experiments. No effort was made to thermally stabilize the system. The largest drift, >20 nm/min, was measured just after loading the sample. In some cases, the drift reduced to less than 2 nm/min. The rotational and scale drifts were found to be less than 0.1 μ rad/min and 2×10^{-8} /min, respectively.

Knowledge of the system drift enables a minimization of absolute pattern-placement errors. For our system in its current configuration, registration to global alignment marks

must be done every minute to keep placement errors, due to system drift, below 10 nm. Such a technique was used in the stitching and overlay experiments reported in Sec. V.

IV. INTRAFIELD DISTORTION MEASUREMENT

Distortion in the electron-beam deflection field leads to systematic pattern-placement errors. This intrafield distortion arises from nonidealities in the electron optics, the beam deflector, and the deflection and field-calibration electronics. The amount and direction of the distortion is typically non-uniform and nonlinear across the field.

To measure these distortions we used an interference-lithography-generated reference grid and follow a method similar to that of Anderson *et al.*⁷ As Anderson and others^{7,8} have shown, high-quality interference lithography can produce reference grids with negligible distortion over the areas of concern for deflection field metrology. For these experiments, a 320-nm-period chromium-on-silicon fiducial grid was used, which provided a low-noise secondary-electron signal.

Initially, the field was calibrated by examining the grid at four locations. The measured phase shift at these four locations determines the necessary field corrections for rotation, scale, and field-shift errors. The proper field-calibration values were then set electronically. To measure the intrafield distortion, the fiducial grid was then scanned at a number of points throughout the field, i.e., an 11×11 array, while the system's stage remained stationary. The center of the field was tracked between measurements of each point in the intrafield array so that the stage and/or beam drift (see Sec. III) could be removed from the data. The measured spatial phase of the grid at each point gave a value of the beam's positional error at that intrafield location. The phase shift was calculated using a Fourier transform of the grid signal, and the position error was determined by $(\phi/2\pi) \Lambda_{\text{GRID}}$, where ϕ is the locally measured spatial phase of the grid and Λ_{GRID} is the grid period. By measuring the phase of an array of marks, rather than the edge or centroid of an individual mark, the uncertainty in beam position can be reduced below the nanometer level. In this manner, a high-precision intrafield-distortion map was compiled rapidly.

The intrafield-distortion map shown in Fig. 4 was acquired for a $100 \mu\text{m}$ field size, an accelerating voltage of 10 kV, and a working distance of about 6.5 mm. Each arrow in the map represents the x - and y -phase measurements of a $3.840 \mu\text{m} \times 3.840 \mu\text{m}$ (12 periods \times 12 periods) scan of the fiducial grid. The measurement locations were separated by $9.600 \mu\text{m}$ (30 periods). The lower-right corner of the field exhibits the maximum deflection error of 15 nm. An alternative intrafield-distortion measurement, made by moving a small mark array to various field locations with the laser-interferometer stage, yielded similar results but with larger measurement variances.

V. OVERLAY AND STITCHING PERFORMANCE

The overlay and stitching performance of the Raith 150 system was evaluated in a set of multilevel patterning experi-

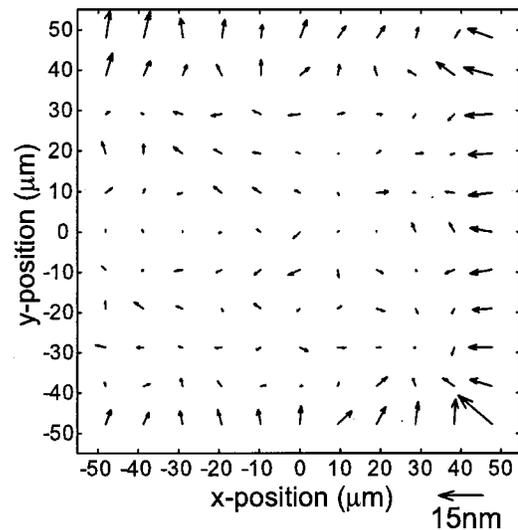


Fig. 4. Map of the Raith's intrafield distortion for a $100 \mu\text{m}$ field. A maximum distortion of 15 nm occurs in the lower-right corner of the field.

ments. Three levels of writing were done for each experiment: patterning of global-registration marks (level 1), patterning of stitched fields, field-registration marks, and the first set of overlay marks (level 2), and patterning of the second matching set of overlay marks (level 3). Performance was evaluated at low- and high-acceleration voltages. Also, two registration techniques were used for the overlay patterning experiments.

Before each level of writing, the substrate's U , V coordinates were mapped and the field size was calibrated carefully. The mapping errors were typically less than 3×10^{-6} in scale and rotation. To minimize field-calibration errors, the Raith's autocalibration routine was executed seven times, and average values were used as the field settings. The uncertainties in these values were found to be about 2×10^{-5} in scale and $25 \mu\text{rad}$ in rotation. The instrument is currently in an acoustically and mechanically noisy environment, 10 m from a road with heavy traffic. Improved field-calibration performance is expected with better vibration isolation.

Global-registration marks were first patterned (level 1) in a single-layer resist at five locations on a bulk silicon wafer. Four marks were located 10 mm apart in a square array, and were used to map the laser-interferometer coordinates X , Y to the wafer coordinates U , V in subsequent writes. A fifth mark was placed at the center of the square. The time to pattern all five marks was about 75 s. The marks were transferred in metal using a liftoff process described in Sec. I. After the liftoff step, the wafer was coated with the single-layer resist as described in Sec. II. Then, resist in an area around each global-registration mark was exposed for its removal in a development step. Thus, the global marks were available for registration in subsequent exposure levels.

The field-stitching marks, field-registration marks, and first set of overlay marks were patterned next (level 2). Four, $100\text{-}\mu\text{m}$ -sized fields were stitched together, and the pattern was repeated 100 times over a 1 cm^2 area. Stitching marks were placed $5 \mu\text{m}$ from the corners of the $100\text{-}\mu\text{m}$ -sized

fields. Their design enabled measurements of stitching to be made parallel and perpendicular to the field boundary. The mark location was chosen to maximize sensitivity to field rotation and scale errors. During this level of writing, overlay marks and field-registration marks were also patterned. The overlay marks were also located $5\ \mu\text{m}$ from the field's corners, and an additional mark was placed at the field center. The field-registration marks were placed $10\ \mu\text{m}$ from the field boundaries (see Sec. IV). Between the patterning of each set of four fields, a registration was made to the central global-registration mark to minimize absolute placement errors. Only a field-shift correction was applied after each global registration. The writing time for the four-stitched-field set was 17 s, and the registration time was at most 15 s for each set. Thus, any placement errors caused by drift were limited to 4 nm. The sample was developed, as described in Sec. II, after this level of writing.

Marks for the second level of overlay writing were patterned last (level 3). Registration for this overlay writing was done using two different methods. The first method was to register only to the central global-registration mark between sets of fields, as was done in the previous writing level. This was done for two fields in the four-field set, and took at most 15 s for the two fields. An advantage of this method is that no real estate is required within each field for registration marks. The second common method was to register, field-by-field, to registration marks within the field. This was done for the remaining two fields in each set. This registration allowed updating of the field-calibration values, and took 4 s/field. Because of the Raith's in-lens secondary-electron detector, sufficient signal contrast was obtained from the field-registration marks patterned in the 50-nm-thick PMMA during the previous writing level. However, at an acceleration voltage of 20 kV, the signal from these marks became unsatisfactory for good registration.

The sample was developed again after the last level of patterning, and then subjected to liftoff processing as described in Sec. II. All marks were transferred in metal to the silicon substrate, and measured approximately 100 nm wide by $2\ \mu\text{m}$ long. The position of these marks could be determined easily using the metrology software of the Raith system. The measurement uncertainty of the mark location was found to be 2.2 nm in a separate experiment.

Figure 5 represents the mean μ and twice standard deviation 2σ placement errors measured for a 20 kV field-stitching experiment. The arrows represent the magnitude and direction of the mean errors, and the bars represent twice the standard deviation for the X and Y scanning directions. A 10 nm scale marker is shown for reference. The dashed lines represent the abutment of the four 100- μm -sized fields. The largest stitching error was $\sim 33\ \text{nm}$, $|\mu| + 2\sigma$. Numerical values for this measurement are summarized in Table I. The Roman numerals I–IV in Table I represent the 1-to-4, 2-to-1, 3-to-2, and 4-to-3 field boundaries, respectively.

At lower acceleration voltages, the mean stitching errors increased while the standard deviations remained about the

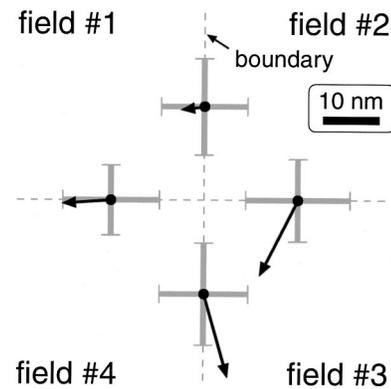


FIG. 5. Field-stitching results at 20 kV. The arrows represent the magnitude and direction of the mean stitching errors measured at four boundaries (shown as dashed lines) near the corners of 100- μm -sized fields. The bars represent twice the standard deviation of the stitching errors. A 10 nm scale bar is shown for reference.

same. At 10 kV, the largest mean error was 34 nm, and at 2 kV the maximum mean error was 68 nm. The larger mean stitching errors at low voltages are believed to be a result of poor field calibration due to stray-field effects on the beam during the calibration procedure.

Although this stitching result at 20 kV over the $1\ \text{cm}^2$ area is quite good, it must be emphasized that a definite time, 17 s, was associated with the writing of the four stitched fields. If the exposure time were longer, then an increase in the mean stitching errors in accordance with the system drift, reported in Sec. III, would be expected. The authors anticipate eliminating this potential problem by implementing spatial-phase-locking techniques⁹ on the Raith 150 instrument.

Results from the overlay measurements at 2 and 10 kV are summarized in Table II. At 20 kV, field registration was not possible due to the poor signal quality from the marks, as noted earlier. Only results from the marks measured at field center are reported, since the results at the field corners were approximately equivalent. At 2 and 10 kV, the performance was better when registration was done using the field-registration marks within each field. This data also show substantially larger pattern-placement errors at the lower voltage. This again is believed to be due to stray-field effects on the beam, i.e., charging in the column, chamber, or on the sample. The best overlay achieved at 10 kV was about 35 nm, $\mu + 2\sigma$.

TABLE I. Numerical values of field-stitching errors, for a 20 kV writing voltage, are listed. The number of trials to obtain the values was 100. See Fig. 5 for a graphical representation of these results.

| | X (nm) | | Y (nm) | |
|-------|--------|----------|--------|----------|
| | μ | σ | μ | σ |
| 20 kV | | | | |
| I | -7.8 | 8.6 | -0.6 | 6.2 |
| II | -2.5 | 7.7 | -0.3 | 8.6 |
| III | -6.9 | 9.3 | -13.7 | 7.3 |
| IV | 4.4 | 7.9 | -15.4 | 9.1 |

TABLE II. Numerical values of overlay errors, for 2 and 10 kV writing voltages, are listed. The improved performance at 10 kV was attributed to a reduction in stray-field effects.

| | Globally registered | | | | Field registered | | | |
|-------|---------------------|----------|--------|----------|------------------|----------|--------|----------|
| | X (nm) | | Y (nm) | | X (nm) | | Y (nm) | |
| | μ | σ | μ | σ | μ | σ | μ | σ |
| 2 kV | 36.1 | 30.5 | -28.4 | 39.6 | 17.2 | 26.2 | 9.6 | 9.0 |
| 10 kV | -34.9 | 14.4 | 13.4 | 14.2 | 18.7 | 8.9 | 1.8 | 6.4 |

By using higher voltages and metallic field-registration marks, better overlay performance may be possible. However, this adds additional processing steps to the substrate's preparation. An alternative approach to improving overlay performance is the application of spatial-phase-locking techniques.⁹

VI. SUMMARY

The Raith 150's resolution, stability, intrafield distortion, overlay and stitching performance were evaluated. Patterning at low- and high-acceleration voltages was compared. The highest patterning resolution and pattern-placement performance were obtained for acceleration voltages above 20 kV.

The system was used to pattern sub-20 nm features, and pattern-placement accuracy below 20 nm, mean plus standard deviation, was demonstrated.

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¹See the Raith 150 Turnkey Electron-Beam Lithography System technical handout for system details (provided by Raith USA, Inc., Islip, NY).

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